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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,483	11/13/2000	Oh-Nam Kwon	8733.307.00	4557

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/709,483	KWON, OH-NAM	
	Examiner	Art Unit	
	Thanh V Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/21/04 has been entered.

Response to Arguments

2. Applicant's arguments filed 05/24/04 have been fully considered but they are not persuasive.

3. Applicant's argument on the substrate of only a single layer is not persuasive. Although support for "single material" is seen in fig. 5, e.g., there is no support for single layer. The prepared substrate on page 5 and subsequent pages of the originally filed specification do not indicate that the substrate is a single layer substrate. Plural portions of the substrate 1 are encompassed by "layer". In light of the original application, the substrate 1 is one of the layers of the substrate as indicated in the previous Final Office action mailed 02/24/04 and the Advisory mailed 06/09/04.

Response to Amendment

Claim Rejections

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this instance, "substrate of only a single layer" is new matter as discussed above.

6. Claims 1-2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matanabe et al. US 5,705,230 in combination with Havemann et al. U.S. Patent No. 5,891,804.

The Matanabe et al. reference discloses an improved method for filling trench in a single layer substrate 5 to produce many kinds of semiconductor devices including contacting or electroconductive parts 3/1, abstract, col. 1, lines 7-14 and figs 3-5. The Matanabe et al. reference skips the steps of forming the photoresist and etching, the forming a second metal with a height being smaller than a depth of the groove and removing the photoresist pattern.

The Havemann et al. reference discloses a process for forming thin film conductors comprising forming a photoresist pattern 46 on a substrate 42/40; etching a portion of the substrate to form a groove 47 *beneath a top surface of the glass substrate* using the photoresist pattern as a mask; depositing a second metal 50 on the substrate, col. 2, lines 13-15, and a height of the second metal being smaller than a depth of the

groove, fig. 3b; removing the photoresist pattern on the substrate and the second metal on the photoresist other than in the grove, fig. 3c; and forming the first metal 52 principally copper, col. 2, line 18, on the second metal in the groove, col. 4, lines 54-55, by electroless plating.

The step of electroless deposition inherently includes the step of preparing a mixed solution having a reductant and a first metal and submerging the substrate in the mixed solution.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method steps of Havemann in the method of Matanabe et al., mainly to the single layer substrate of Matanabe et al., as those formation steps would have been selected to improve further the filling trench in accordance with the thin film conductor as taught by Matanabe et al.

7. Claims 4-5, 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination as applied to claims 1-2 and 11 above, and further in view of Senda et al. U.S. Patent No. 5,364,459.

Re claims 1-2 and 11, the combination discloses essentially all of the limitation, it does not disclose Ag and Au and the kind of reductant used.

Re claims 2, 4-5, 7-8, 10-11, the Senda et al. reference discloses in the background of the invention that the first metal could be Cu, Ag or Au; the reductant could be formaldehyde; and "the electroless plating is not only applied to formation of a conductive film such as an electrode for an electronic component", col. 1, lines 10-35.

It would have been obvious to one of ordinary skill in the art to apply the known materials as stated by Senda et al. to the method of the combination because such materials would have been chosen for electroless plating process in order to have better trench fill in the art of making electrode for an electronic device. The use of Cu, Ag or Au and formaldehyde is well known to those skilled in the art as taught by Senda et al.

8. Claims 3, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann et al., Matanabe et al. and Senda et al. as applied to claims 1-2, 4-5, 7-8 and 10-11 above, and further in view of Charneski et al. U.S. Patent No. 6,284,652 B1 and/or Eriksson U.S. Patent No. 3,632,435.

Both Havemann et al./Matanabe et al. and Senda et al. do not disclose the mixed solution for the electroless plating.

The Charneski et al. reference discloses sulfuric acid and cupric sulfate (col. 8, line 31) used in cooper plating process.

The Eriksson reference discloses the use of silver nitrate, gold chloride with noble metal salts and hydroxide in the mixed solution for electroless plating (col. 5, lines 45-65).

It would have been obvious to one of ordinary skill in the art to apply the known materials as stated by Charneski et al. and/or Eriksson to the method of Havemann et al./Matanabe et al. and Senda et al. because such materials would have been chosen for the electroless plating process in the art of making electrode for an electronic device in the process of the combination of Havemann et al. and Senda et al. The use of

sulfuric acid and cupric sulfate is well known to those skill in the art as taught by Charneski et al. and/or Eriksson.

9. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann et al./Matanabe et al. and Senda et al. as applied to claims 1-2, 4-5, 7-8, 10 and 11 above, and further in view of JP 05-265040 and applicant's admitted prior art.

The Havemann et al. reference discloses a process for forming thin film conductors comprising forming a photoresist pattern on a substrate using electroless plating, the Senda et al. reference discloses formation of a conductive film such as an electrode for an electronic component using electroless plating.

None of the references disclose the further steps for forming the transistor.

However, JP 05-265040 (provided by applicant) discloses the steps of making gate line in a trench and the applicant admitted prior art that performing the further steps for forming the transistor.

It would have been obvious to one of ordinary skill in the art to apply the gate electrode of Senda et al. using the method of Havemann et al./Matanabe et al. into of making a trench gate line and the applicant's admitted prior art of forming transistor as the method and the analogous electrode would be selected in accordance with JP 05-265040 and the applicant's admitted prior art.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TvP
08/12/04

George Fourson
Primary Examiner